In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A method for adjusting input clock timing affecting performance of data input operations of an integrated circuit comprising the steps of:

successive testing data input operation with an incrementally delayed input clock until all input operations pass;

determining target state programming bits to set the least input clock delay passing the input operation test;

writing the target state of programming bits into a write once memory; and

controlling input clock delay corresponding to said programming bits stored in the write once memory.

2. (Original) The method of claim 1, further comprising:

after determining the target state programming bits and before writing the target state programming bits into the write once memory

storing the target state programming bits in a read/write memory,

testing a non-memory portion of integrated circuit while controlling input delay clock corresponding to the target state programming bits stored in the read/write memory,

determining if the non-memory portion fails the test, and

incrementally delaying the input clock and repeating said steps of storing, testing and determining until the non-memory portion passes the test.

3. (Original) The method of claim 1 wherein:

said step of writing the target state of programming bits into the write once memory includes

applying a programming voltage to each programming bit whose target state is a first digital state,

determining whether each programming bit whose target state is the first digital state reads as the first digital state, and

applying the programming voltage to each programming bit whose target state is the first digital state but which reads a second, opposite digital state,

repeating said steps of determining and applying the programming voltage to each programming bit whose target state is the first digital state but which reads the second digital state until all programming bits whose target state is the first digital state read as the first digital state.

4. (Original) The method of claim 1 wherein:

said step of writing the target state of programming bits into a write once memory includes writing programming bits not related to data input operations performance.

5. (Original) The method of claim 4 wherein:

the programming bits not related to data input operations performance include an identification code of a specific die.

6. (Original) The method of claim 1 further comprising the steps of:

successive testing data output operation with an incrementally delayed output clock until all output operations pass;

determining output target state programming bits to set the least output clock delay passing the output operation test;

writing the output target state of programming bits into the write once memory; and

controlling output clock delay corresponding to said programming bits stored in the write once memory.

7. (Original) A method for adjusting output clock timing affecting performance of data output operations of an integrated circuit comprising the steps of:

successive testing data output operation with an incrementally delayed output clock until all output operations pass;

determining target state programming bits to set the least output clock delay passing the output operation test;

writing the target state of programming bits into a write once memory; and

controlling output clock delay corresponding to said programming bits stored in the write once memory.

8. (Original) The method of claim 7, further comprising:

after determining the target state programming bits and before writing the target state programming bits into the write once memory

storing the target state programming bits in a read/write memory,

testing a non-memory portion of integrated circuit while controlling output clock delay corresponding to the target state programming bits stored in the read/write memory,

determining if the non-memory portion fails the test, and

incrementally delaying the output clock and repeating said steps of storing, testing and determining until the non-memory portion passes the test.

9. (Original) The method of claim 7 wherein:

said step of writing the target state of programming bits into the write once memory includes

applying a programming voltage to each programming bit whose target state is a first digital state,

determining whether each programming bit whose target state is the first digital state reads as the first digital state, and

applying the programming voltage to each programming bit whose target state is the first digital state but which reads a second, opposite digital state,

repeating said steps of determining and applying the programming voltage to each programming bit whose target state is the first digital state but which reads the second digital state until all programming bits whose target state is the first digital state read as the first digital state.

10. (Original) The method of claim 7 wherein:

said step of writing the target state of programming bits into a write once memory includes writing programming bits not related to data input operations performance.

11. (Original) The method of claim 10 wherein:

the programming bits not related to data input operations performance include an identification code of a specific die.

12 to 20. (Canceled)